TITLE: hardware Implementation of Neural Networks (CS)
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DESCRIPTION: A software library is to be developed for implementing neural networks in Gate Array (hardware) form, commencing with the ubiquitous Multi-Layer Perceptron/BackPropagation architecture. The user will specify the number of input, hidden and output nodes. The inherently parallel and re-configurable nature of Gate Arrays is well suited to implementing trainable (adjustable) weights between the network layers. Support for other Neural Net architectures will be investigated if time permits. (PC-based) Xilinx GA software will be provided; likewise background material on NNs if needed. This project would suit someone with prior experience of and/or interest in digital/logic gate and/or finite state machine design, although the Xilinx tools come equipped with an alternative VHDL (i.e. HLL) design facility.

DELIVERABLE: A C++ library to enable the high-level design of evolvable hardware (specifically NNs) using the Xilinx development platform. An ambitious student might even relish the challenge of developing a 'hardware compiler' interface to the pre-existing Xilinx tools.